The Argument For Indium Solder in Cryogenics & Quantum Grade Packaging

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Abstract

The pursuit of scalable quantum computing has increasingly turned to photonic systems as a viable pathway, leveraging the inherent advantages of light-based information processing. In photonic device packaging, indium has become as a critical material for die attach due to its unique combination of softness, ductility, and low melting point [1]. Its high thermal and electrical conductivity and low melting point allow dies to be attached at low temperatures in order to avoid damaging sensitive photonic components. This makes indium suitable for applications that require precise alignment and minimal mechanical stress on optical dies.

Introduction

AmTECH Microelectronics, a provider of custom microelectronics and photonics packaging services in Silicon Valley, has proven to play a critical role in the development of photonic packaging systems. AmTECH has been tasked with the process development of a package that includes; a photonic integrated circuit (PIC), low-noise amplifier (LNA) dice, and a variety of other miniature components. To address these packaging requirements, the team has utilized advanced bonding tools sourced from Finetech, Hesse Mechatronics, and Centrotherm. The utilization of this equipment has included the use of various materials including formic acid, nitrogen, and indium preforms. Indium solder is one of the most reliable interconnect or interface material in cryogenic systems due to its persistent ductility, excellent wetting, and ability to accommodate thermal mismatch and cycling [1]. Its unique mechanical and thermal behavior makes it a default choice for engineers developing technology in the quantum, aerospace, or deep cryogenic research applications. This reliability, especially in low-temperature environments, makes indium a key material for next generation quantum grade packaging.

Plasma Cleaning

As we walk through the process, the initial steps are to purge the materials of any contaminants. The substrate, die, and Indium are prepared in order to minimize moisture, remove oxidations, and eliminate organics. This focus on preparing the materials prior to reflow is key in attaining a high-quality bond with minimal voiding. Eliminating voiding is necessary as it increases the strength of the bond and assures proper heat transfer. These two factors are key considerations for this application. One of the main elements with regards to preparation is the use of plasma cleaning. This process utilizes a controlled mixture of oxygen and argon to remove contaminants from the material surfaces. The overall cleaning procedure plays a critical role in ensuring successful bond-ability and maintaining a low voiding concentration.

Vacuum Reflow

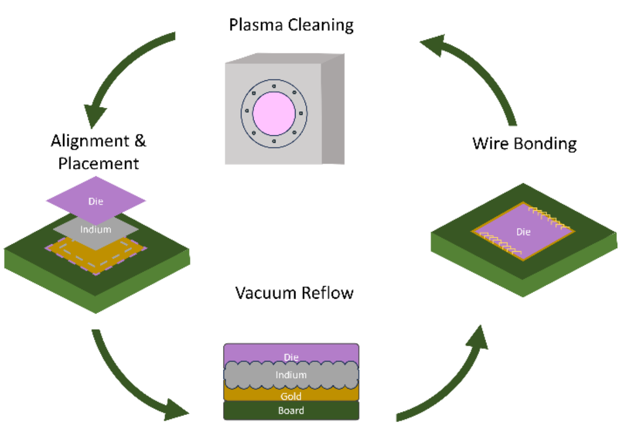

Figure 1: Process flow diagram depicting vacuum reflow eutectic die bonding, illustrating key steps.

Vacuum reflow involves the development of an inert environment using nitrogen, and a process gas that is used to reduce oxidation and ensure a clean metallic bond. The process gas is used to help strip away contaminants which eliminates the need for traditional flux. This process ensures that the bonding surfaces remain pristine, facilitating optimal adhesion and electrical conductivity. To avoid compromising the integrity of the sensitive structures required for photonic devices, the process development prioritized low-temperature bonding conditions. Selecting the optimal material for the process was a critical part of the process development flow. Indium ultimately being chosen as it has a melting point of 157 degrees Celsius and highly ductile properties. Likewise, the chosen processing gas, formic acid, has shown evidence of performing well at temperatures below 200 degrees Celsius.

After conducting plasma cleaning, both indium and die placement are enabled and regulated by custom fixtures. These fixtures are used to control the position and apply precise pressure on the dies in order to control and aid in the bonding process. Once the indium, die, and fixture are properly aligned they are placed inside the processing chamber of AmTECH's vacuum reflow oven in order to begin the vacuum reflow process. The machine uses a profile to precisely control vacuum pressure, gas flow, and temperature.

The process begins by drawing vacuum in order to create an evacuated environment to reduce the probability of enabling oxidation. After the vacuum phase the chamber is then pumped with nitrogen in order to create an inert environment. The nitrogen stage is followed by another vacuum stage in order to ensure no oxygen remains within the vacuum reflow chamber. After the second vacuum phase is complete the chamber is filled with formic acid. The chamber then heats up to just below the liquidous temperature of the indium before pausing and allowing for the formic acid to clean. After this pause, the chamber heats up to a high temperature in order to guarantee that indium is in its liquidous state. During this phase the vacuum is pulled once more to remove any air bubbles in the indium in order to mitigate the formation of voids . After resting at 185 degrees for several minutes the cooling process begins by using a combination of nitrogen and water to cool down the machine. After the cooling cycle, the fixture is removed and the part undergoes a quality control phase.

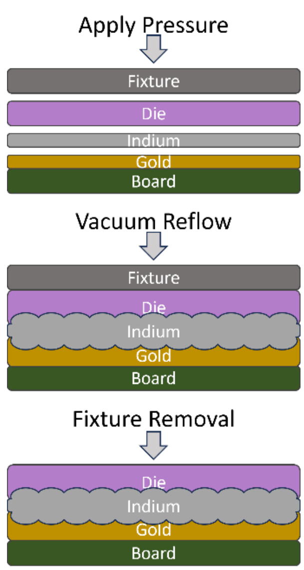

Figure 2: Side profile illustration of the eutectic die bonding process, showing sequential steps The process enables uniform bonding of the die to the gold-coated substrate using indium solder**.**

The quality control phase includes X-ray testing to determine void concentration.

The x-ray testing is used to determine the quality of the bond by looking for areas of voiding. Based on these results, we can assess whether the bond meets the minimum requirements outlined in AmTECH's quality control protocol.

When the quality control phase is complete the final phase would be the completion of a high-precision wire bonding operation. This is done using the Hesse Mechatronics platform. The machine’s large work area allows for bigger substrates to be bonded making it advantageous when comparing it to its counterparts. The wire bonding step is critical for establishing robust electrical interconnects between the substrate and low-noise amplifier (LNA) components. To assess bond reliability, 3–5% of wire bonds are subjected to destructive pull testing, providing statistical validation of mechanical robustness.

Results

A manual die attach process was performed using the same die and indium material to provide a direct comparison with the vacuum reflow results.

Continuous void analysis after vacuum reflow is conducted ensuring optimal process performance and long-term device reliability.

This characterization technique enable a direct comparison between the manual die attach process and the vacuum reflow method.

Below are X-ray images of the die bonds from the manual die attach, unoptimized vacuum reflow process, and optimized vacuum reflow process.

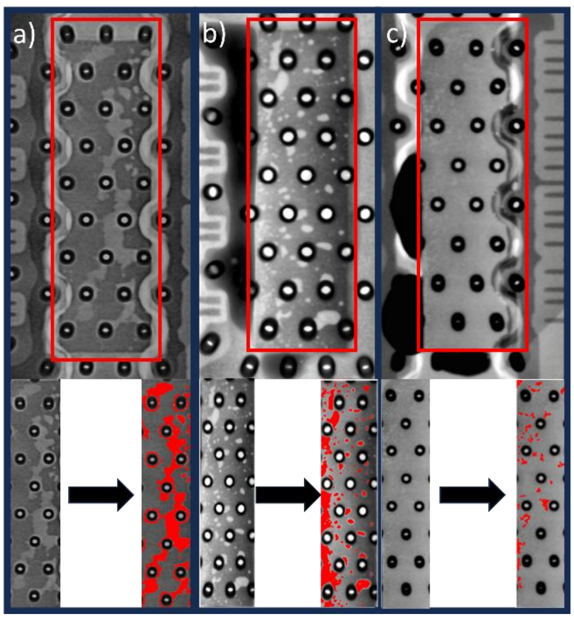

Figure 3: Top images show the raw X-ray scans with red rectangles outlining the die bond regions. The bottom row highlights the analyzed area used for void quantification. Void percentages were calculated using an image processing algorithm for **(a)** manual die attach (25.29%), **(b)** unoptimized vacuum reflow (15.94%) **(c)** optimized vacuum reflow (4.86%).

All die bond regions were processed using a image analysis script that quantified the percentage of voided areas based on grayscale contrast. The script identified voids by segmenting regions with distinct intensity differences from the surrounding material. It then calculated the total voided area as a percentage of the die bond region to enable quantitative comparison across samples.

Figure 3a displays the X-ray images of the die bond region for the manual die attach technique. This resulted in 25.29% voided area. According to the IPC-A-610 standards [2] this is somewhat acceptable. The IPC-A-610 standard states that voiding must be less than or equal to 25% per solder joint [2].

Figure 3b shows the die bonds produced by the vacuum reflow die attach process prior to profile optimization, resulting in a voided area of 15.94%. Following process optimization, the void percentage was significantly reduced to 4.86%, as shown in Figure 3c. These results demonstrate a substantial improvement in void reduction compared to both the unoptimized vacuum reflow process and the manual die attach technique.

Voiding in the manual die attach process likely resulted from trapped air, uneven adhesive application, or outgassing during curing without controlled pressure or environment. Vacuum reflow is designed to minimize voids by applying heat and vacuum to evacuate trapped gases. However process conditions can still lead to significant voiding if not properly controlled.

Summary

Vacuum reflow eutectic die bonding has proven to be an effective process for achieving reliable, and low-void attachment of photonic components quantum computing platforms. Leveraging indium solder and a carefully controlled sequence of plasma cleaning, inert gas purging, and formic acid vapor treatment, this process enables clean, uniform metallic bonds while operating at low temperatures suitable for thermally sensitive photonic integrated circuits (PICs). When compared to conventional manual die attach methods the vacuum reflow approach significantly reduces void formation and enhances mechanical strength, as highlighted in the x-ray inspection.

The combination of plasma surface preparation, precise fixture alignment, and advanced vacuum reflow technology provides a scalable and repeatable solution for complex photonic packaging challenges. By mitigating voids and ensuring high bond integrity, this process supports the reliability demands of high-performance quantum

systems. Furthermore, the successful integration of high-precision wire bonding complements the overall assembly, reinforcing electrical interconnect robustness. These advancements position vacuum reflow indium bonding as a promising candidate to become the industry standard for next-generation photonics packaging.

Sources

[1] Zhang, Q., Dusek, A., & Kuehn, J. (2006). Reliability assessment of indium solder for low temperature electronic packaging. In 2006 8th Electronics Packaging Technology Conference (EPTC) (pp. 224–229). IEEE. https://www.researchgate.net/publication/253038904_Reliability_assessment_of_indium_solder_for_low_temperature_electronic_packaging

[2] IPC-A-610 standards